REMARKS

This paper responds to the Office Action mailed on July 17, 2006.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

§103 Rejection of the Claims

Claims 11-25, 35-39 and 41-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "INTEGRATED CIRCUITS - Design Principles and Fabrication" (1965 textbook) taken with DEVICE ELECTRONICS for INTEGRATED CIRCUITS (1986 textbook), in view of Yamada (U.S. 5,266,528) along with (U.S. 5,408,739). Applicant traverses.

The cited 1965 textbook discloses sawn die that have active areas and inactive areas. Applicant respectfully submits that there is nothing in the reference to suggest bringing the edge of the scribe lane close to the edge of the active area, and points to the section indicated by the Examiner (summary point 8 on page 162) to show that the reference teaches away from bringing the scribe edge close to the active area, since point 8 states that you should "Maintain a minimum die size", which one of ordinary skill would understand means keeping the die large enough to contain the isolation regions, bonding pads, and interconnect area. That the use of the term maintain has this meaning may be further understood with reference to the summary point 4, which shows that the reference uses the term "Minimize" when referring to shrinking an area. Thus, Applicant submits that the cited reference teaches against the present claimed invention.

The cited 1986 textbook discusses the history of IC miniaturization and Applicant can find nothing to suggest reducing the size of the non active region of the die. The portion of the text indicated by the Examiner does not show sufficient detail to have any suggestion of flatter smoother scribe edges.

The cited Yamada patent discloses sawing scribe lanes using a diamond embedded resin saw blade. There is no disclosure in the cited reference regarding the distance of the edge of the scribe lanes 2 from an edge of an active region, which is not mentioned in the reference. The cited reference requires two cut operations with different width blades, different diamond mesh size, and different feed speeds, to form the scribe cut.

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Title: GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS

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U.S. 5,408,739 (to Altavela) is used in the outstanding Office Action to show that further polishing may not be required to obtain a smooth surface. Altavela discloses sawing the front surface of a thermal ink jet printer head so that the sawing leaves a front surface that does not require a polishing step (see Fig. 8 and col. 1, lines 7-14). However, Applicant respectfully submits that there is not proper motivation given to combine an ink jet reference with a saw reference to obtain a ground or polished surface with a specific location relative to the active circuitry area. Further, the disclosed procedure of Altavela requires two saw cuts, one from the front side and one from the back side to obtain a single face. Altavela does not suggest separating the "die" from the wafer with the disclosed process, but rather forming a print head surface.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the feature of "...with a top portion of each individual planar perimeter side surface disposed in the second region and within 5 microns of an edge of active circuitry in the first region...", as recited in independent claim 11, as amended herein. The other independent claims recite similar language, and are therefore also not suggested by the combination of references. The cited references do not provide any disclosure or suggestion of a scribe edge within 5 microns of active devices as recited in claim 11 and the other independent claims.

The dependent claims are felt to be in patentable condition at least as depending from base claims shown above to be patentable over the references. In light of the above noted claims amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

AARON M. SCHOENFELD

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 349-9587

Date

Timothy B. Clise

Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this ______ day of November 2006.

KATO GALLOW

16/10/100

Signature

Name